Low-Voltage PLL

A Low-Voltage PLL with a Supply-Noise Compensated Feedforward Ring VCO – TCAS-II

Block Diagram



250 ps 50 mV ↓

연세대학교

ONSEI UNIVERSITY

Chip Microphotograph



Performance Summary

Performance Parameters	This work
Technology (nm)	180
(Nominal Supply Voltage)	(1.8 V)
Supply Voltage (V)	0.65
Core Area (mm ²) *	0.0075 **
Output Freq. (GHz)	0.4
Phase Noise @ 1-MHz offset (dBc/Hz)	-90.3
RMS Jitter (ps)	13.1 (0.0052 UI)
Power (mW)	0.14 **
Power Efficiency (mW/GHz)	0.35 **

Jitter Measurement Results



Jitter Peaking Result





1

Low-Voltage PLL

• A Low-Voltage PLL with a Current Mismatch Compensated Charge Pump – ISOCC

Block Diagram



Chip Microphotograph



Jitter Measurement Result



Performance Summary

Technology [nm]	180
Supply [V]	0.65
Frequency [MHz]	400
Area [mm²]	0.0075
Power [µW]	140

Reference Spur with Compensation





Phase Noise Measurement Result





Low-Power Transmitter

- A 0.202-0.333 pJ bit, 5-8 Gb/s Transmitter with 2-Tap Pre-Emphasis Based on Data Toggle Information
 - \rightarrow International patent pending



